

# A 1-Gb/s/pin 512-Mb DDRII SDRAM using a digital DLL and a slew-rate-controlled output buffer

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## Abstract

We developed a 1-Gb/s/pin 512-Mb DDRII SDRAM composed of a digital delay-locked loop (DLL) and a slew-rate-controlled output buffer. The digital DLL has a frequency divider for the DLL input, which performs at a operating frequency of up to 500 MHz at 1.6 V, and it provides internal clocking with 50% duty-cycle correction. The DLL has a current-mirror-type interpolator, which enables a resolution as high as 14 ps, is standby-current-free, and can operate at voltages as low as 0.8 V. The slew-rate impedance-controlled output buffer circuit reduces the output skew from 107 to 10 ps. This SDRAM was tested using a 0.13- $\mu$ m 126.5-mm<sup>2</sup> 512-Mb device.

## 1. Introduction

The design of computer systems is constantly improving both in terms of performance and power consumption, and the 1.8-V DDRII SDRAM is one solution for the main memory [1]. However, because interfaces with such a DDRII memory have a higher data rate, it is difficult to maintain a valid data window at a low operating voltage. We developed a DDRII SDRAM that features clock regeneration with duty-cycle correction, fast restart to depress the standby current, and precise skew control. This 512-Mb DDRII SDRAM has new circuits including (1) a low-power digital DLL with a duty-cycle corrector and (2) an output buffer circuit to adjust the impedance and slew-rate.

## 2. Digital DLL circuit with a duty-cycle corrector

The DLL is shown in Figure 1. The input clock (CLK1) frequency has been divided. This expands the operating frequency of the DLL, the replica of the DQ buffer, and the phase detector (PD) effectively to double. In addition, this reduces the operating current by half.

The I-DLL block is used to align the output data timing with the input clocking, and the H-DLL block is used to produce tCK (clock-cycle time)/2 delay for 50 % duty-cycle correction. Each block has two variable delay lines (VDLs) to obtain the same delay time.

The coarse delay line (CDL) is composed of n-stage delay lines consisting of eight units of two inverters with a TAP driver (Fig. 2). The upper bits of the counter codes (S3-9) select two adjacent TAPs (e.g., TAPE1k-TAPO1k, TAPO1k-TAPE2k, ...) and output FDLE and FDLO [2]. The fine delay line (FDL) interpolates between FDLE and FDLO (Fig. 3) [3]. The lower bits of the counter codes (S0-S2) determine switches and provide currents I1 and I2: Here, I2 is proportional to binary-weighted code S0-2, and I1 + I2 is constant. When S0-S2 = "000", I2 is zero, and, hence, I2' is zero. Thus, only the rising FDLO discharges OUTB linearly. As the code increases, FDLO and FDLE discharge OUTB under the ratio allocated by I1' and I2', respectively. Because the circuit is composed of current mirrors, the two-inverter delay is interpolated with good linearity.

The lock-in sequence of the DLL is described in Figure 5. Here, tDL represents the delay time between CLK and RCLK for the I-DLL, and that between CLK1 and CLKHF for the H-DLL. The I-DLL locks when the rising RCLK is consistent with the rising CLK. First, the counter increments by eight CDL units (16 inverters) every eight cycles from 5.4-ns tDL, even if the decrement may be faster to reach at a lock-in point. When tDL exceeds a lock-in point, the counter begins to decrement by a unit, which is followed by FDL adjustment. Accordingly, the I-DLL locks at the optimum cycle. The lock-in tDL is 1, 2, and 3 times tCK, when tCK is 8.0, 3.75, and 2.0 ns (500 MHz), respectively.

The duty-cycle correction is described in Figure 4. If tDL of the H-DLL corresponds to the tCK/2 lock mode only, the operating frequency is limited to 250 MHz, because the initial tDL is 2.0 ns. The frequency divider can triple the operating frequency in the 3/2tCK lock mode. The H-DLL locks as the rising CLKFBH agrees with the falling CLK1. Since both clocks are frequency-divided, the delay tDL is (odd number)  $\times$  tCK. Hence, the final tDL is tCK/2 or

3/2tCK; not 1 tCK. The maximum frequency of the delay line is calculated to be up to 750 MHz. The optimum lock mode is selected automatically without complicated control for both the DLL blocks. The non-DCC mode (the output duty equals the input CLK duty) is implemented by switching VDL input to CLKB1.

Figure 6 shows the waveforms of simulated DLL signals at 500 MHz, 1.6 V. The digital DLL operates in a range from 66 to 500 MHz (1 Gb/s). The suspension of the unused delay line by CDLMBk, the frequency divider, and the low voltage (1.6 V) reduce the operating current to 29 mW at 266 MHz. Since the interpolator has a low gain, the DLL starts quickly with the input receiver. This reduces the active power down-current, ICC3P, (and the active non-power down-current, ICC3N, in some cases) to almost zero. In addition, the DLL can operate at voltages as low as 0.8 V because of the low gain of the interpolator. Table 1 summarizes DLL features.

## 3. Slew-rate and impedance-controlled output buffer circuit

To obtain a high-speed interface such as one faster than 1 Gb/s/pin, the output skew must be eliminated. A DDRII SDRAM has impedance control of the output driver, which is shown in Figure 7. It can provide suitable output impedance for various memory systems; however, it cannot control the output slew rate and the output skew caused mainly by the device characteristics and temperature fluctuation. In the conventional slew-rate and impedance-control scheme [4], the slew-rate is controlled by coordinating the gate level, which used MOS capacitors, of both the base driver and the supplemental drivers to adjust the output impedance. However, this scheme has a problem not only with power dissipation caused by large capacitors, but also with a large output capacitance, which impedes high-speed switching in system buses, because supplemental drivers need the structure of two series large transistors to control the slew-rate. Our scheme can solve these problems, which is shown in Figure 8. In our scheme,  $\phi$  1-6 signals control PMOS and NMOS impedance independently. The slew-rate is controlled on the base buffer only. This is because supplemental drivers do not significantly affect the slew-rate. Therefore, this scheme can easily reduce the output capacitance and eliminate the output skew. Figure 9 shows simulated waveforms of DQ outputs. The output skew was reduced to less than 10 ps which is without slew-rate control.

## 4. Implementation of the 512-Mb DDRII SDRAM

Figure 10 shows a microphotograph of the chip of the 512-Mb DDRII SDRAM. Table 2 summarizes the chip specifications. A 4-bit pre-fetch system was used in the DDRII operation. This SDRAM has four banks, and each bank is split into four 32-Mb array blocks. Each 32-Mb array is composed of 16  $\times$  8 sub-array blocks of 512 cells/WL, 256 cells/BL.

## 5. Summary

We developed a 512-Mb DDRII SDRAM to test a memory interface with a 1-Gb/s data rate. The locking frequency of the digital DLL circuit ranged from 66 to 500 MHz at 1.6 V, and the DLL can operate at voltages as low as 0.8 V. The output circuit reduced the output skew to less than 10 ps by adjusting the impedance and slew-rate.

## Acknowledgments

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## References

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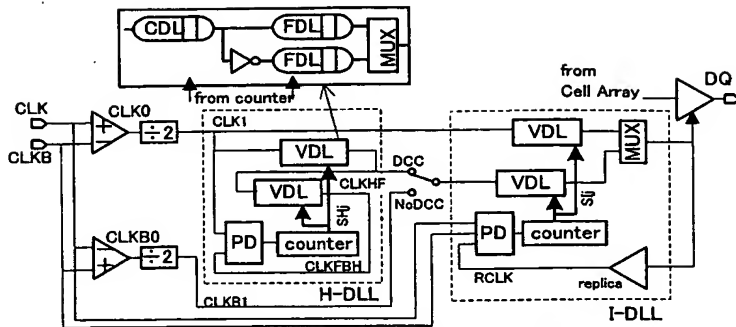


Fig. 1 Block diagram of DLL circuit.

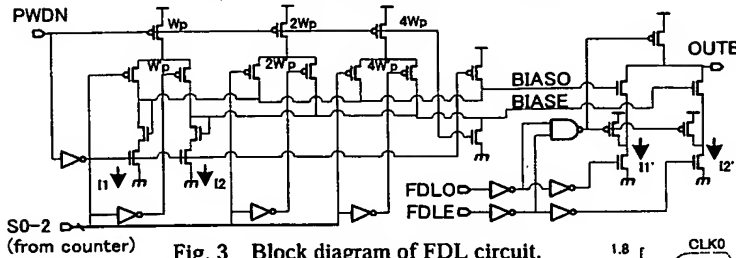


Fig. 3 Block diagram of FDL circuit.

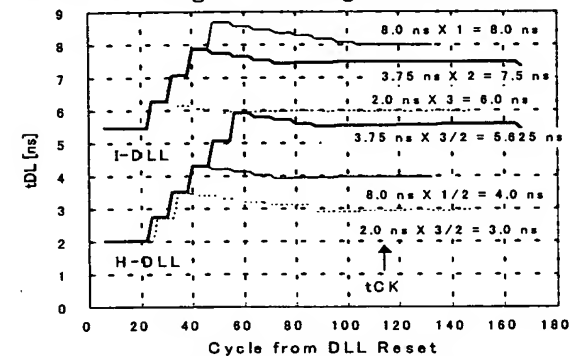


Fig. 5 DLL locking simulation.

Table 1 DLL features.	This Work	DDR-II Requirement	DDR-I Requirement
Operating Voltage	> 0.8 V	1.8 V	2.5 V
Operating Frequency	66 - 500 MHz	125 - 400 MHz	66 - 166 MHz
Resolution	14 ps	50 ps	70 ps
Active Power (ICC4)	29 mW	~ 40 mW	~ 50 mW
Standby Power			
in bank activated (ICC3P)	< 0.1 mW	2 ~ 40 mW	2 ~ 50 mW
in bank idle (ICC2P)	< 0.1 mW	2 ~ 10 mW	2 ~ 10 mW

\*1: 5 % of the access-time window

Table 2 Chip specifications.

Process	0.13 $\mu$ m triple-metal CMOS
Chip Size	10.73 mm X 11.79 mm (126.5 mm <sup>2</sup> )
Package	60-pin CSP
Organization	4 bank, X4/X8
Voltage	1.8 V(per.)/1.6 V(DLL)/1.4 V(array)
Interface	SSTL18
Refresh	8 k/64 ms

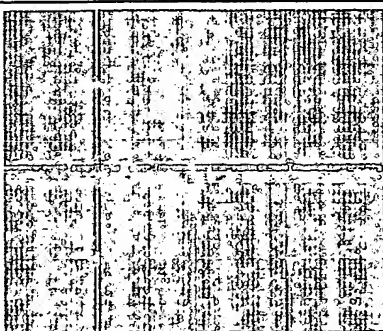


Fig. 10 Chip microphotograph.

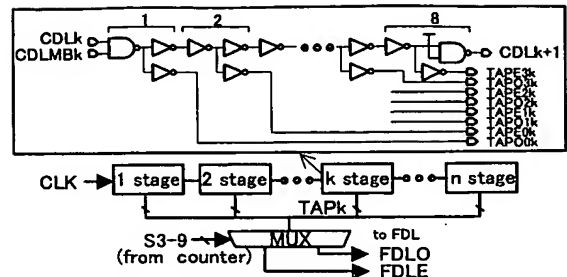


Fig. 2 Block diagram of CDL circuit.

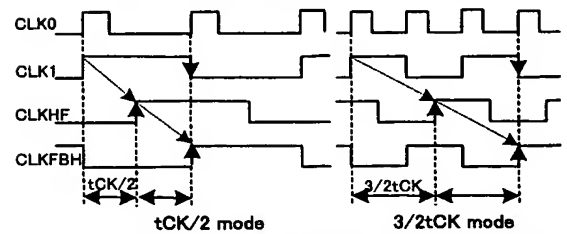


Fig. 4 Timing diagram of tCK/2 and 3/2tCK modes.

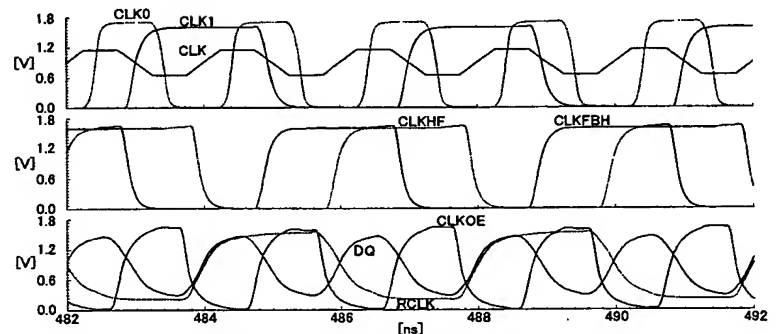


Fig. 6 Waveforms of simulated DLL signals.

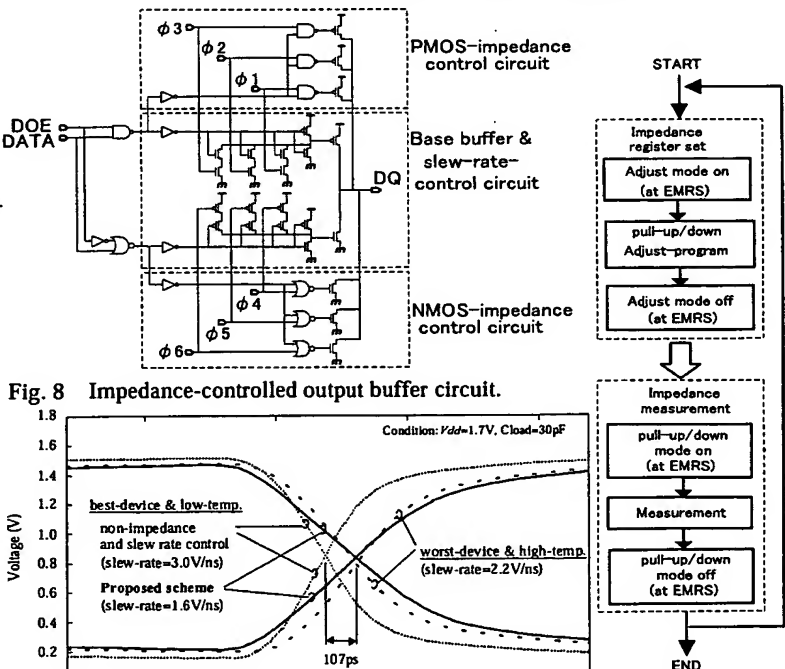


Fig. 8 Impedance-controlled output buffer circuit.

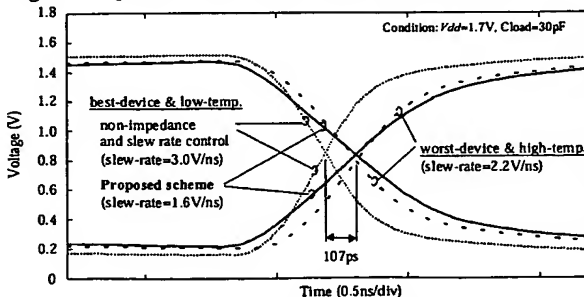


Fig. 9 Simulated waveforms of DQ outputs.

Fig. 7 Impedance adjustment.

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